Code: 15O-9304 **ECE**

THIAGARAJAR POLYTECHNIC COLLEGE, SALEM
(Autonomous) **Reg. No.** |_____|

October/November 2019 Examinations
DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING
Advanced Communication Systems

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 Define RADAR.
2 Mention the types of aircraft landing system.
3 What is an ASCII code?
4 Mention any two advantages of optical fiber.
5 Define splice and connector in optical fiber.
6 Mention any two types of microwaves devices.
7 Define the term frequency reuse.
8 List different types of satellite orbits.

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Mention any three applications of RADAR.
10 State the features of ISDN.
11 Explain Baud Rate.
12 Define scattering losses and mention its types.
13 Explain Kepler's first law.
14 Describe about transponders with necessary diagram.
15 Mention important types satellite multiple access technique.
16 Define coupler and mention the various types of couplers.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All questions carry equal marks.

17 A Explain the working of the pulsed RADAR system with neat block diagram. 10

(OR)

B i) Explain Cylindrical Scanning in facsimile sender. 10
ii) Explain synchronization in facsimile receiver.

18 A Explain the digital communication system with a block diagram. 10

(OR)

B Explain the working of PSK Modulator and De Modulator with waveforms. 10

19 A Explain in detail about absorption losses and bending losses. 10

(OR)

B Explain any two applications of optical fiber with necessary diagrams. 10

20 A With the block diagram, explain transmit receive earth station. 10

(OR)

B Explain travelling wave tube with neat block diagrams. 10

21 A Explain in detail about simplified cellular telephone system with necessary diagrams. 10

(OR)

B Explain GSM system architecture with neat block diagram. 10

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October/November 2019 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Microcontroller

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 What is the function of program counter in 8051?
2 What will happen after the execution of instruction DIV AB?
3 What are the instructions used to access external RAM in 8051?
4 What is the capacity of bit addressable area of internal RAM in 8051?
5 Give the format of TMOD register in 8051.
6 What is mode 1 of serial communication in 8051?
7 What is meant by interrupt priority?
8 What is the need of ADC interfacing?

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Draw the PSW register format.
10 What is meant by assembler directive? Explain it with two examples.
11 Write an 8051 program to toggle bit 5 of PORT1 continuously.
12 Write a program for getting the data from PORT1 and send it to PORT2.
13 What is RS232? Draw the interfacing of RS232 with 8051.
14 Explain the use of IE register.
15 Write the control word format of 8255.
16 Compare microprocessor and microcontroller.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All questions carry equal marks.

17 A Draw the architecture of 8051 and explain the function of each block. 10

(OR)

B Draw and explain the pin configuration of 8051. 10

18 A Write short notes on : 10
(i) Structure of Assembly language
(ii) Assembling and Running on 8051 program.

(OR)

B Write an 8051 program to arrange the given set of numbers in descending order. 10

19 A Explain in detail about the programming of timer. 10

(OR)

B Write about the operating modes of timer/counter with neat diagram. 10

20 A How will you program the 8051 to transfer and receive data serially? 10

(OR)

B Explain the programming of external hardware interrupt and serial communication interrupt. 10

21 A Draw the block diagram of 8255 and explain the modes of operation. 10

(OR)

B Explain seven segment LED display interfacing with 8051. 10

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THIAGARAJAR POLYTECHNIC COLLEGE, SALEM

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October/November 2019 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Very Large Scale Integration

Year/Sem: III/V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 Simplify the expression using Boolean's theorems Y= AC + A'BC .
2 What are Races in digital circuits? List their types.
3 What is logic synthesis?
4 Write the VHDL code for OR gate.
5 What is state diagram?
6 Compare Latch and FF.
7 What is ASIC? List its types.
8 Draw the state diagram for MOD 2 counter.

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Synthesis the function Y= A'B'C' + A'BC' + AB'C' + ABC'.
10 Synthesis Half Adder using Demultiplexer.
11 What is physical design in the design process of VLSI?
12 Compare Mealy and Moore FSM.
13 Write the VHDL code for TFF with reset input.
14 Compare PLA with PAL.
15 What are FPGA and CPLD?
16 Write the VHDL code for 2 to 1 MUX.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All questions carry equal marks.

17 A Realize NOT and NOR gates using CMOS. 10

(OR)

B Implement the function Y= ∑(1,2,3,5,7,10,13) with minimal gates and multiplexer. 10

18 A Explain the process of VLSI design flow using CAD tools. 10

(OR)

B Develop the VHDL code for four bit arithmetic adder with block diagram and Full Adder logic diagram. 10

19 A Explain the operation of SISO and SIPO shift registers with suitable diagrams. 10

(OR)

B Design Moore FSM for MOD 6 counter using D FF with suitable state diagram. 10

20 A Develop VHDL code for D Flip Flop's with & without reset input. 10

(OR)

B Develop the VHDL code for decade counter with logic diagram and truth table. 10

21 A Implement the function of Full Subtractor in PAL. 10

(OR)

B Implement the function Y=∑(0,1,2,5,6,7,8,11,14,15) in PLA. 10

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THIAGARAJAR POLYTECHNIC COLLEGE, SALEM

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October/November 2019 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Programmable Logic Controller

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 State any two advantages of automation.

2 Expand the term FBD and STL.

3 What is ladder diagram?

4 What is TOF instruction?

5 What is the use of 'High Speed Encoder'?

6 List down the various data manipulating instructions used in PLC.

7 What is meant by Full duplex communication mode?

8 List the name of any two market available PLC.

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Write notes on PLC scan.

10 Compare PLC circuit versus hardwired circuits.

11 Why do we need timer instructions?

12 What is the function of RTO instruction?

13 What is the purpose of PID instruction?

14 Draw the configuration of Sourcing output module.

15 What is the necessity of TTL output module?

16 Write short note on XIO instruction.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question. (ii) All questions carry equal marks.

17 A Draw and explain the block diagram of PLC system. 10

(OR)

B i) What are the applications of PLC? 10
ii) Explain the types of PLC's.

18 A Explain the following instructions 10
a) Examine ON b) OTE
c) OTL d) OSR (One Shot Rising)

(OR)

B i) Develop ladder logic diagram for the logic gates : AND , OR , XOR and NAND 10
ii) Draw and explain the ladder logic diagram of Multiplexer.

19 A Draw a ladder diagram for a two motor system having the following conditions 10
i) The start switch starts motor 1 first, after 15s motor 2 starts.
ii) The stop switch stops motors 1 and 2.

(OR)

B What is a CTD instruction? Explain its working with the help of suitable ladder diagram and timing diagram. 10

20 A List down the various comparison instructions used in PLC & explain each briefly. 10

(OR)

B Develop the ladder logic diagram for conveyor belt system and explain the rung in the ladder diagram. 10

21 A Explain the function of AC Discrete input modules with neat diagram. 10

(OR)

B i) Briefly Explain 'IEEE 488 BUS' 10
ii) List the advantages and disadvantages of Star topology.

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