Code: 15O-9304 **ECE**

THIAGARAJAR POLYTECHNIC COLLEGE, SALEM

(Autonomous) **Reg. No.** [ ]

October/November 2018 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Advanced Communication Systems

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 List the types of RADAR display.

2 Define simplex and duplex.

3 Expand ASCII and EBCDIC.

4 Name any two error correction codes.

5 What is critical angle?

6 Define Apogee and Perigee.

7 Expand CDMA and FDMA.

8 What is Roaming?

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Draw the block diagram of Pulsed Radar System.

10 Briefly explain about Hamming code.

11 List the difference between single mode and multi mode fibre.

12 Define Connectors, Splices and mention its types.

13 State and explain Kepler's first law.

14 Briefly explain about Transponders.

15 Briefly explain the basic concept of Bluetooth technology.

16 Draw and explain ASK modulator.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All divisions carry equal marks.

17 A Explain the architecture of ISDN system with neat sketch. 10

(OR)

B Draw and explain the schematic diagram of Instrument Landing System (ILS). 10

18 A Explain the basic elements of digital communication system with neat diagram. 10

(OR)

B Draw the block diagram of QPSK modulator and explain each block in detail. 10

19 A Draw the block diagram of optical communication. What are the advantages of optical communication? 10

(OR)

B Define Couplers and list its types. Explain any two types of couplers used in optical fibre. 10

20 A Draw and explain Geostationary synchronous orbit and mention its advantages. 10

(OR)

B Explain the microwave link repeater in detail with neat diagram. 10

21 A Explain the simplified cellular telephone system with necessary diagrams. 10

(OR)

B Sketch the architecture of GSM system and explain its operation. 10

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October/November 2018 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Microcontroller

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 What is the use of program counter?
2 Write any 4 bit manipulation instructions.
3 Mention the various steps used for assembling an ALP.
4 What is the function of **C/$\overline{T}$** bit in TMOD register?
5 What are the bit addresses of Port 2 ?
6 Explain serial port control register.
7 What is 8255?
8 Draw the interfacing diagram of relay with 8051.

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Write the different Logical Instructions . Explain any 2 with example.
10 Explain stack and stack pointer .
11 Define assembler directive and explain any two.
12 Write an ALP to multiply two 8-bit numbers.
13 Explain BIT and BYTE addresses of RAM structure.
14 Explain mode 0 of T/C operation.
15 Write about the different modes of serial data communication.
16 Write the different modes of operation of 8255.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All divisions carry equal marks.

17 A Explain the memory organisation of 8051. 10

(OR)

B Describe the classifications of 8051 instruction set. 10

18 A Explain assembling and running of a program in 8051. 10

(OR)

B Write an ALP to find the biggest number from 5 nos. 10

19 A Explain I/O Programming. 10

(OR)

B Explain in detail about the different modes of timer operation. 10

20 A Explain the programming steps to transmit and receive data serially using 8051. 10

(OR)

B Explain the programming of external hardware interrupts. 10

21 A Explain how external memory is interfaced with 8051. 10

(OR)

B Explain in detail about stepper motor interfacing. 10

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October/November 2018 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

VERY LARGE SCALE INTEGRATION

Year/Sem: III / V (ODD -III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 Draw the logic diagram of OR gate using NMOS.
2 Draw the logic diagram of NOT gate using CMOS.
3 Write the VHDL code for AND gate.
4 Define multiplexer.
5 What are the four conditions exist in a flip flop?
6 Write the VHDL code for T flip flop.
7 Expand the term FPGA.
8 Draw the truth table of D flip flop.

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Draw the logic diagram of NOR gate using NMOS.
10 Explain circuit synthesis using gates
11 List out any four logical operators.
12 List out any four assignment statements.
13 Explain state diagram.
14 Explain state table.
15 Write the VHDL codes for storage elements.
16 Write the difference between PLA and PAL.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All divisions carry equal marks.

17 A Explain circuit synthesis using MUX and DEMUX. 10

(OR)

B Implement the function $F=\sum(0,2,4,7)$ with minimal gates. 10

18 A Develop a VHDL code for encoder and decoder. 10

(OR)

B Develop a VHDL code for DEMUX. 10

19 A Design a 3 bit counter using D flip flops with proper excitation table and state diagram. 10

(OR)

B Design a mod-5 counter using D flip flops with proper excitation table and state diagram. 10

20 A Develop a VHDL code for implementing a JK flip flop. 10

(OR)

B Develop a VHDL code for implementing a Johnson counter. 10

21 A Implement the function $F=\sum(1,5,7,11,13,14,15)$ in PROM and PLA. 10

(OR)

B Explain FPGA with diagram. 10

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Code: 15O-9401A **ECE**

THIAGARAJAR POLYTECHNIC COLLEGE, SALEM

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October/November 2018 Examinations

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

Programmable Logic Controller

Year/Sem: III / V (ODD-III) Max. Marks : 75 Time : 3 hr.

PART-A **(5 x 2 = 10 Marks)**

Note: (i) Answer any FIVE questions out of which question No.8 is compulsory.
(ii) All questions carry equal marks.

1 What are the major parts of a PLC?
2 What is meant by unitary PLC?
3 Expand: i) SFC (ii) STL
4 Develop ladder logic for OR gate.
5 What is Time base in Timer?
6 What is meant by preset in counter instruction?
7 Expand the term PID.
8 What is IEEE 488?

PART-B **(5 x 3 = 15 Marks)**

Note: (i) Answer any FIVE questions out of which question No. 16 is compulsory.
(ii) All questions carry equal marks.

9 Draw the block diagram of PLC.
10 State the differences between PLC and computer.
11 Write short notes on Function block diagram.
12 Explain the characteristics of PLC Timer.
13 Explain the functions of PLC Counter.
14 Explain different addressing types of Micrologic PLC.
15 What are the classifications of I/O Module?
16 Develop program using statement list for AND gate & OR gate.

PART-C **(5 x 10 = 50 Marks)**

Note: (i) Answer all the questions choosing either sub-division (A) or sub-division (B) of each question.
(ii) All divisions carry equal marks.

17 A With neat sketch explain the elements of power supply unit of PLC. 10

(OR)

B With neat sketch explain about PLC scan. 10

18 A Develop and explain the ladder logic for XOR, NAND and NOR gates. 10

(OR)

B Develop ladder logic to demonstrate 4:1 Multiplexer. 10

19 A With the help for timing diagram explain the sequence of operation of TON instruction. 10

(OR)

B With the help of timing diagram explain the sequence of operation of CTD instruction. 10

20 A Explain various mathematical instructions. 10

(OR)

B Briefly discuss about the concept of PID instruction. 10

21 A With neat sketch explain the working of DC Discrete input module. 10

(OR)

B Briefly discuss about various communication mode. 10

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